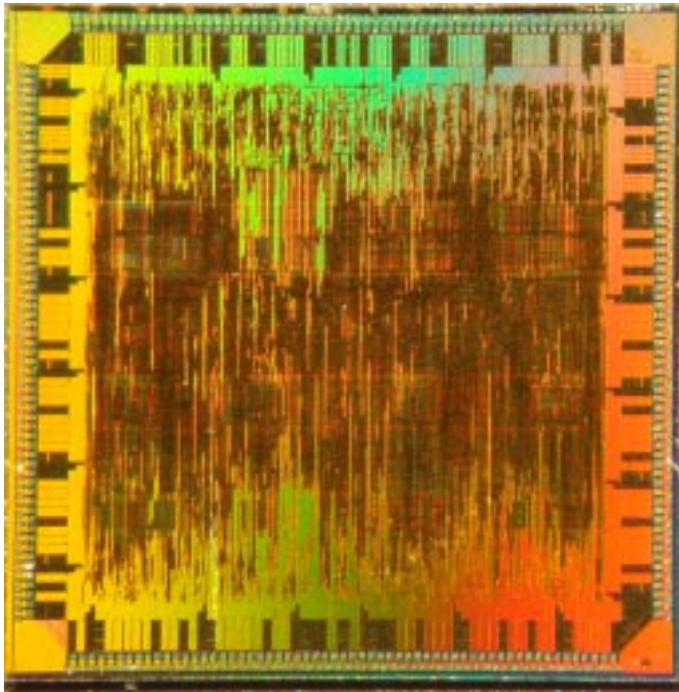
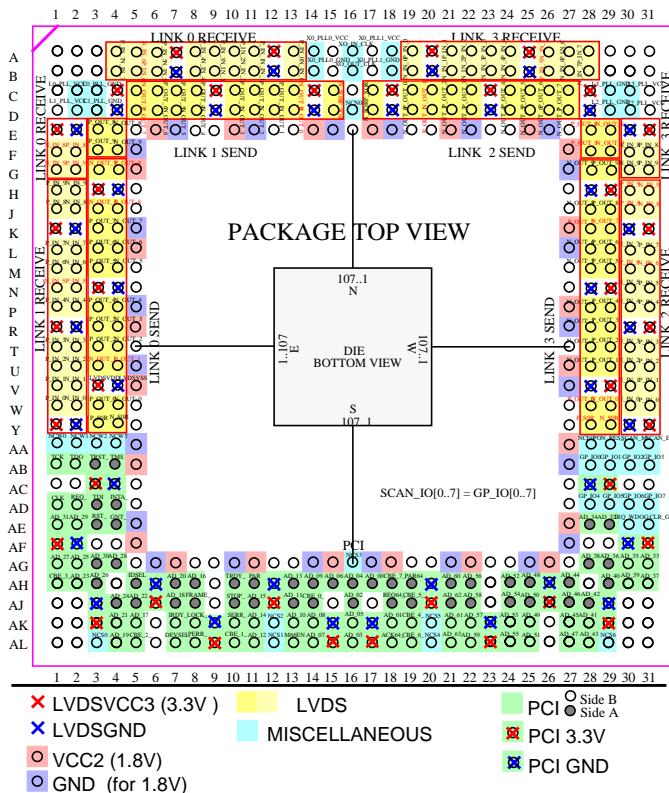


the ATOLL chip

a network on a chip



DIE photo of the 5,7 x 5,7 ATOLL chip



BGA ball out optimized for 4 layer PCB board

Universität Mannheim
 Lehrstuhl für Rechnerarchitektur
 Prof. Dr.-Ing. Ulrich Brüning
 Tel. 0621 181 2723 Fax 0621 181 2713
<http://www.atoll-net.de>

The highly integrated CMOS ATOLL-Chip is the basic building block for an ATOLL-SAN.

The ATOLL development tries to optimize the price/performance ratio of the network interface controller by implementing all required components (host interface, host ports, network interfaces, switch, link interfaces) for a SAN on a single chip (except the link cables) combined with very innovative architectural features at a price/performance range not yet achieved.

It is a complete network on a chip including the self-routing 8 x 8 crossbar. Only the ATOLL chip on a PCI board and two cables are required to build scalable cluster systems.

The chip contains approx. 4.5 Mio. Transistors in 0.18 μ m technology from UMC.

It is a standard cell design based on a highly automated design flow. The design time was only 3 man years.

The chip features:

- 5.7 x 5.7 die size
- 4.5 Mio. Transistors in 0.18 μ m technology
- 250MHz typical clock frequency
- power consumption of only 5W
- 440 staggered I/O pads
- 520 ball custom BGA package
- custom I/O cells for PCI-X
- custom LVDS with integrated termination resistors
- PCI-X high speed bus interface (64bit @ 133MHz)
- 4 byte-wide bidirectional LVDS links
- 2GBytes/s interconnection network bandwidth

The ATOLL clock generation is optimized for performance and cost. Every ATOLL chip has an integrated clock oscillator controlled by an external crystal of 14.318 MHz, which is the cheapest precise clock base to be installed. The on-chip clock frequency is generated from a PLL which can be programmed in the range from 114 to 501 MHz, depending on the speed grade of the chips in a cluster. The typical operating frequency of ATOLL will be 250MHz and all ATOLL chips of a cluster must be operated at approximately the same frequency.

Link data transmission is performed on 9 differential signal lines and one differential clock line, requiring 2 x 20 wires for one bidirectional link. The maximum cable length is 4 m.